Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (currently amended) An integrated circuit chip with multiple wirebonds, comprising:

a semiconductor substrate;

a transistor in and on ~~over~~ said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a second contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over said first contact pad and exposes said first contact pad, and wherein a second opening in said passivation layer is over said second contact pad and exposes said second contact pad;

a power metal structure over said passivation layer and on said first contact pad, wherein said power metal structure is connected to said first contact pad through said first opening, wherein said power metal structure comprises a copper layer, and wherein one of said multiple wirebonds is bonded on said power metal structure;

a ground metal structure over said passivation layer and on said second contact pad, wherein said ground metal structure is connected to said second contact pad through

said second opening, wherein said ground metal structure comprises a copper layer, and wherein another one of said multiple wirebonds is bonded on said ground metal structure;

a capacitor over said passivation layer and directly over said first contact pad exposed by said first opening;

a first solder connection connecting said capacitor to said power metal structure; and

a second solder connection connecting said capacitor to said ground metal structure.

2-3. (canceled)

4. (withdrawn) The integrated circuit chip according to claim 1 further comprising a polymer layer over said passivation layer, wherein said power and ground metal structures are on said polymer layer.

5-6. (canceled)

7. (currently amended) The integrated circuit chip according to claim 1, wherein said ground metal structure further comprises a gold layer over said copper layer of said ground metal structure.

8. (canceled)

9. (currently amended) An integrated circuit chip comprising:

a semiconductor substrate;

a transistor in and on ~~over~~ said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over ~~exposing a~~ said first contact pad and exposes said first contact pad, ~~of said multiple metal and dielectric layers,~~ and wherein said passivation layer comprises nitride;

a second contact pad connected to said first contact pad through said first opening, wherein the position of said second contact pad from a top perspective view is different from that of said first contact pad, and wherein said second contact pad comprises a gold layer with a thickness greater than 1 micrometer;

a capacitor over said passivation layer and over said second contact pad; ~~and~~

a solder connection between said capacitor and said second contact pad, wherein said solder connection connects ~~connecting~~ said capacitor to said second contact pad; and~~.~~

an additional metal layer between said solder connection and said second contact pad.

10. (previously presented) The integrated circuit chip according to claim 9 further comprising a third contact pad exposed by a second opening in said passivation layer, and a wirebond on said third contact pad.

11. (previously presented) The integrated circuit chip according to claim 9 further comprising a third contact pad over said passivation layer, and a wirebond on said third contact pad.

12. (previously presented) The integrated circuit chip according to claim 9 further comprising a third contact pad exposed by a second opening in said passivation layer, a fourth contact pad on said third contact pad, and a wirebond on said fourth contact pad.

13-14. (canceled)

15. (currently amended) An integrated circuit chip with a wirebond, comprising:

a semiconductor substrate;

a transistor in and on ~~over~~ said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a first contact pad over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers, wherein a first opening in said passivation layer is over said first contact pad and exposes said first contact pad;

a second contact ~~first metal~~ pad connected to said first contact pad through said first opening; ~~over said semiconductor substrate;~~

a third contact ~~second metal~~ pad connected to said first contact pad through said first opening and connected to said second contact pad, wherein the position of said third

contact pad from a top perspective view is different from that of said first contact pad, ~~having a portion over said passivation layer,~~ and wherein said wirebond is bonded on said third contact pad; ~~second metal pad is used to be wirebonded thereto;~~

a capacitor over said passivation layer and over said second contact pad; and

a solder connection between said second contact pad and said capacitor, wherein said solder connection connects ~~connecting~~ said capacitor to said second contact ~~first metal~~ pad.

16. (canceled)

17. (currently amended) The integrated circuit chip according to claim 15, wherein said second contact ~~first metal~~ pad comprises a gold layer.

18. (currently amended) The integrated circuit chip according to claim 15, wherein said second contact ~~first metal~~ pad comprises a copper layer.

19. (currently amended) The integrated circuit chip according to claim 15 further comprising a ground metal structure connected to said capacitor, to said wirebond and to said first contact pad.

20. (canceled)

21. (currently amended) The integrated circuit chip according to claim 15 further comprising a power metal structure connected to said capacitor, to said wirebond and to said first contact pad.

22. (currently amended) The integrated circuit chip according to claim 15, wherein said second contact ~~first metal~~ pad is over said passivation layer.

23-24. (canceled)

25. (previously presented) The integrated circuit chip according to claim 15, wherein said passivation layer comprises silicon nitride.

26. (canceled)

27. (currently amended) The integrated circuit chip according to claim 15, wherein said third contact ~~second metal~~ pad comprises gold.

28. (canceled)

29. (withdrawn - currently amended) The integrated circuit chip according to claim 15 further comprising a polymer layer over said passivation layer, wherein said second contact ~~first metal~~ pad is on said polymer layer.

30. (withdrawn) The integrated circuit chip according to claim 29, wherein said polymer layer comprises polyimide.

31. (currently amended) The integrated circuit chip according to claim 15 further comprising a polymer layer over said passivation layer, wherein ~~an~~ a second opening in said polymer layer ~~exposing~~ is over said second contact ~~first metal~~ pad and exposes said second contact pad.

32-90. (canceled)

91. (previously presented) The integrated circuit chip according to claim 1, wherein said passivation layer comprises silicon nitride.

92-95. (canceled)

96. (currently amended) The integrated circuit chip according to claim 1, wherein said ground metal structure further comprises a nickel layer over said copper layer of said ground metal structure.

97. (currently amended) The integrated circuit chip according to claim 1 further comprising a polymer layer over said power and ground metal structures, wherein a third ~~first~~ opening in said polymer layer is over ~~exposing~~ said power metal structure and exposes said power metal structure, and a fourth ~~second~~ opening in said polymer layer is over ~~exposing~~ said

ground metal structure and exposes said ground metal structure, said first solder connection connecting said capacitor to said power metal structure through said third ~~first~~ opening, said second solder connection connecting said capacitor to said ground metal structure through said fourth ~~second~~ opening.

98. (previously presented) The integrated circuit chip according to claim 9, wherein said capacitor comprises a decoupling capacitor.

99. (previously presented) The integrated circuit chip according to claim 9, wherein said passivation layer comprises silicon nitride.

100. (canceled)

101. (previously presented) The integrated circuit chip according to claim 15, wherein said capacitor comprises a decoupling capacitor.

102. (currently amended) The integrated circuit chip according to claim 15 further comprising a polymer layer over said passivation layer, ~~an~~ wherein a second opening in said polymer layer is over ~~exposing~~ said third contact ~~second metal~~ pad and exposes said third contact pad.

103. (previously presented) The integrated circuit chip according to claim 102, wherein

said polymer layer comprises polyimide.

104-107. (canceled)